Multilevel Storage in N-Doped Sb_2Te_3-Based Lateral Phase Change Memory with an Additional Top TiN Layer

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In this study, we present the physical images of multilevel storage (MLS) in both vertical and lateral phase change memory (PCM) devices and investigate MLS in a lateral PCM device with an additional top heater (LTH-PCM). The active layers above two lateral electrodes consist of a 50-nm-thick TiN layer as a top heater and a 150-nm-thick N-doped Sb_2Te_3 layer. A number of distinct intermediate levels are obtained by current sweeping or pulse application. According to our analysis, MLS in our devices results mainly from the gradual crystallization between electrodes by Joule heating. © 2009 The Japan Society of Applied Physics

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1. Introduction

There is a growing demand for nonvolatile memory nowadays. One of the most effective methods of increasing the memory capacity is multilevel storage (MLS), by which much more information can be stored without increasing memory size. The application of the phase change memory (PCM)[1–8] based on amorphous–crystalline transitions to MLS is expected since intermediate resistance levels are possible by controlling the total crystallinity between electrodes.[9–13]

However, most current PCMs with a single phase change chalcogenide layer and an in-series heater exhibit sharp resistance changes with the programming pulse amplitude,[2,14] which makes them very difficult to apply to MLS in a stable and controllable manner.

To obtain gradual (or staircaselike) resistance change characteristics, PCMs with stacked chalcogenide layers were proposed and they exhibited MLS potential. However, the number of resistance levels depends strongly on the number of chalcogenide layers, and resistance levels of no more than four have been demonstrated up to now owing to the difficulty in design.[10,15]

In this study, we demonstrate the possibility of MLS using a lateral N-doped Sb_2Te_3 (SbTeN)-based structure (LTH-PCM) with the aid of a top heating layer of TiN. The number of distinct resistance levels can readily reach eight and even higher, depending on programming current.

2. Binary and Multilevel Storage in PCM

2.1 Binary storage in PCM

By applying a high and short electrical pulse between two electrodes of the PCM cell to heat the phase change layer of PCM to a temperature higher than the melting point (T_m) and then quench it, it would be amorphized and the device enters a highly resistive amorphous state as "0" in binary storage. On the other hand, the phase change layer of PCM would be crystallized, and thus, the device would enter a conductive crystalline state as "1" in binary storage if we apply a low and long electrical pulse through filament formation induced by electric field and Joule heating. The reversible phase transformation in PCM is schematically shown in Fig. 1(a). By applying a voltage higher than threshold voltage (V_t), the resistance of the PCM device changes suddenly owing to amorphous-to-crystalline phase transformation. A schematic current–voltage (I–V) curve is shown in Fig. 1(b) to explain this sudden phase change induced by voltage application.

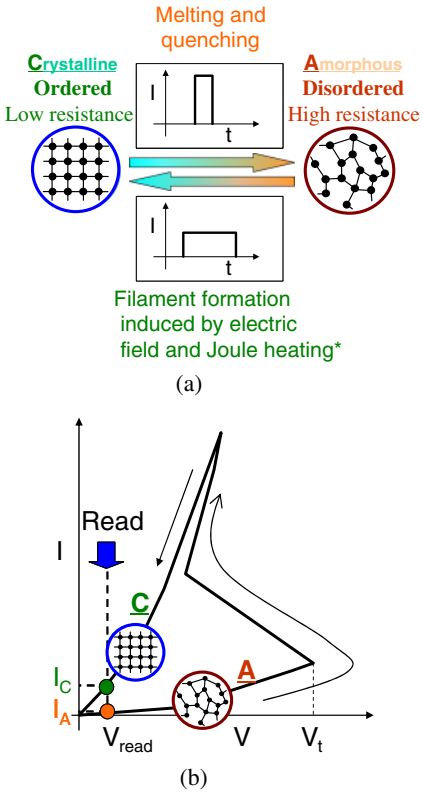

Fig. 1. (Color online) (a) Schematic diagram of phase change in binary storage PCM devices. (b) Schematic diagram of I–V characteristics of binary storage PCM devices.

2.2 Multilevel storage in PCM

Multilevel storage is possible for a PCM device because of the huge resistivity difference between the amorphous and crystalline phases of chalcogenides. As shown in Fig. 2(a), amorphization might gradually proceed with some strategies in a vertical PCM device. The region near the top of bottom electrode contact can have the highest temperature distribution, and it is, therefore, expected that this region will completely be amorphized firstly when a suitable pulse is applied to the device. A higher pulse would enlarge the amorphous region and reduce the crystallinity between two electrodes. Similarly, the enlargement of the amorphous region and the reduction in crystallinity could happen in a

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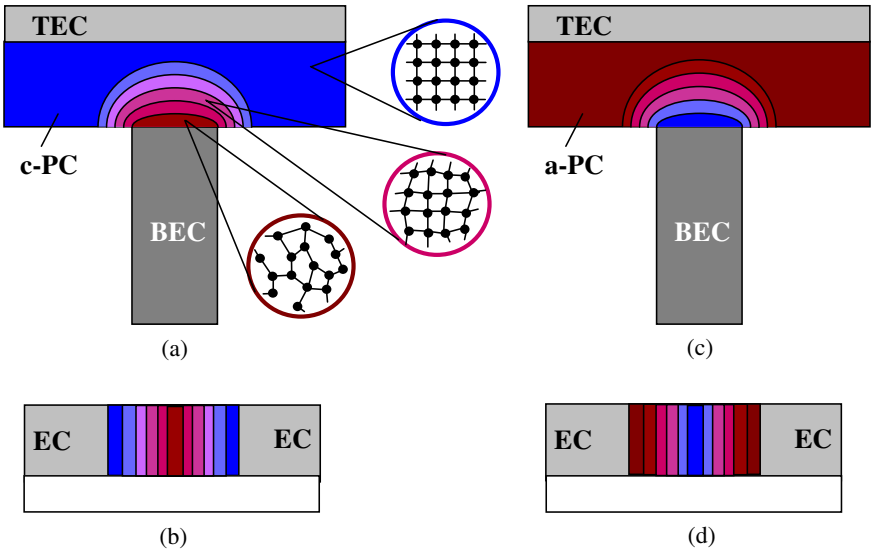

Fig. 2. (Color online) Schematic diagrams of phase change in multilevel storage PCM devices. (a, b) Schematic diagrams of enlargement of amorphous region and reduction in crystallinity between two electrodes in vertical and lateral PCM devices, respectively. (c, d) Schematic diagrams of enlargement of crystalline region and increase in crystallinity between two electrodes in vertical and lateral PCM devices, respectively.

lateral PCM device, as shown in Fig. 2(b). On the other hand, a gradual crystallization might occur with some strategies, as shown in Figs. 2(c) and 2(d). A well-controlled amorphization or crystallization makes a gradual resistance change possible by varying some parameters such as amplitude and duration of electrical pulse.

However, simple structures with a single chalcogenide layer often exhibit a sharp resistance change by pulse application without any strategies.[16] In other words, no well-controlled resistance change is observed for multilevel storage without any strategies. Therefore, strategies of programming or improvements of PCM structures become necessary for the good controllability of resistance change. In this paper, we report a novel simple structure for obtaining a better resistance change controllability.

3. Experimental Methods

Figure 3(a) shows the schematic cross-sectional diagram of our fabricated devices. The active layers of the LTH-PCM device consist of a 150-nm-thick N-doped Sb_2Te_3 layer and an additional top 50-nm-thick TiN layer. The SbTeN and TiN layers were both deposited using a radio frequency sputtering machine (ULVAC MNS-3000-RF) at a sputtering pressure of 0.2 Pa. The Sb_2Te_3 and Ti targets were used during sputtering. N_2 and Ar gases were simultaneously introduced into the chamber during sputtering for doping N into chalcogenide and heater materials. For the SbTeN film, gas flow rates of N_2 and Ar are 1 and 14 sccm, respectively. Amorphous and crystalline SbTeN films have resistivities of around 9×10^{1} and 4×10^{-3} Ω cm, respectively. SbTeN shows a gradual resistivity change above 110 °C.[17,18] For the TiN film, gas flow rates of N_2 and Ar are 2 and 8 sccm, respectively. The TiN film has a resistivity of around 2×10^{-3} Ω cm. Figure 3(b) shows the scanning electron microscopy (SEM) image of the fabricated device.

I–V characteristics of the devices were measured using a semiconductor parameter analyzer (Agilent 4155B). Device resistance was read out at a low current (e.g., 0.02 mA).

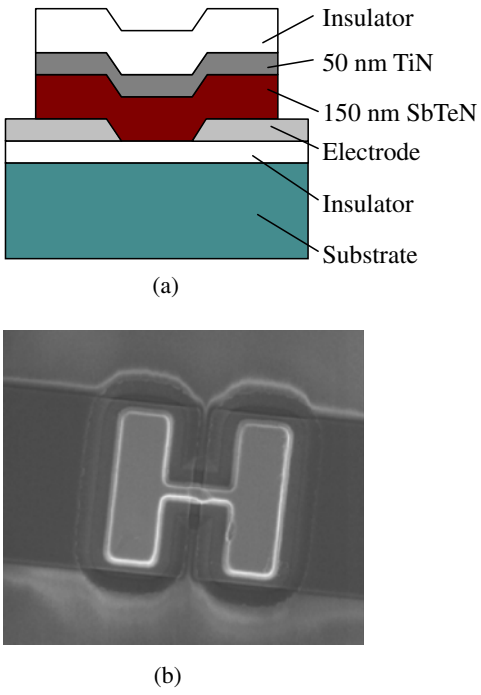

Fig. 3. (Color online) (a) Schematic cross-sectional diagram of our fabricated lateral PCM device with an additional top TiN heating layer. (b) Top view SEM image of the device.

4. Results and Discussion

Figure 4(a) shows the programming characteristics of the device by current sweepings from 0 to the programming currents I_p. The programming currents were 0.5, 1, 2, and 3.5 mA, respectively. The resistance change with programming current is shown in Fig. 4(b). It can be observed that the intermediate levels were very stable because the changed resistance levels can be retained until the sweeping current became higher than the former programming current. In particular, the resistance can be determined by the stop current. For example, current sweeping up to 1 mA resulted

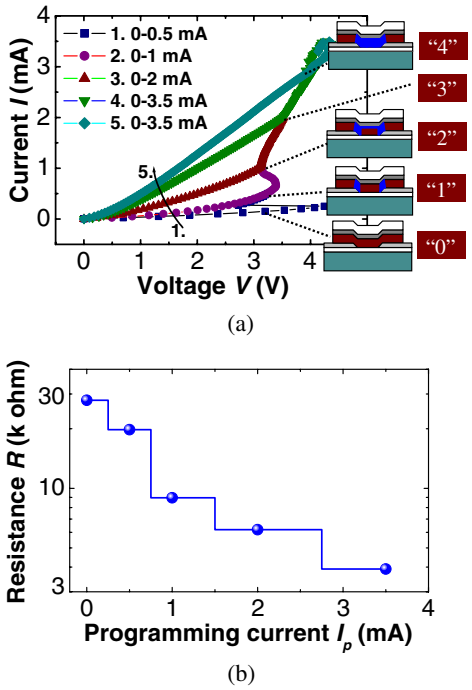

Fig. 4. (Color online) (a) Typical *I*–*V* characteristics of the LTH-PCM device for MLS. (b) Relationship between resistance and programming current, showing staircaselike characteristics.

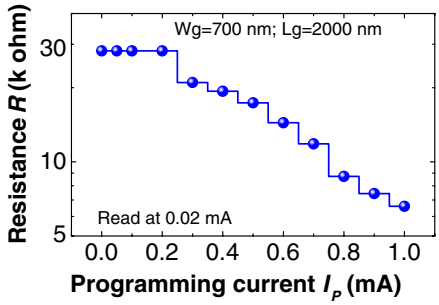

Fig. 5. (Color online) Device resistance drop induced by applied current pulses.

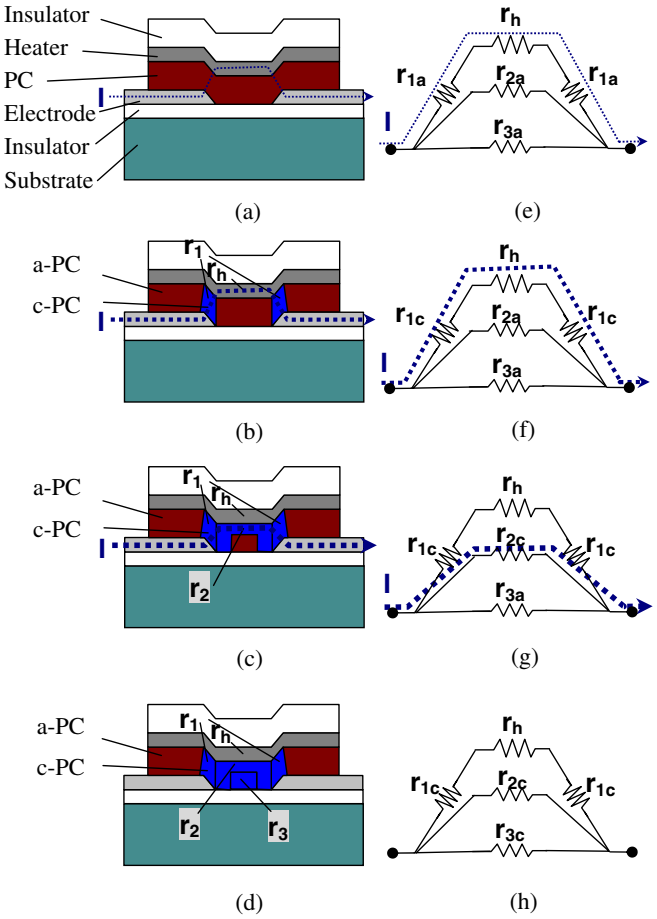

Fig. 6. (Color online) Schematic diagrams of operation mechanism in LTH-PCM device. (a) High-resistance amorphous state. (b) Intermediate-resistance level with crystalline regions induced by an electric field above the threshold field. (c) and (d) Resistance levels with enlarged crystalline regions driven by Joule heating. (e–h) Equivalent circuits corresponding to (a–d), respectively.

in an intermediate resistance of around 9 kΩ. The resistance–programming current (R–I_p) curve in Fig. 4(b) shows three distinct intermediate levels, allowing five-level storage (from level "0" to level "4"). The corresponding schematic diagrams are shown here to better understand the control of cystallinity between two electrodes. These diagrams are shown in Fig. 6 in detail. It should be noted that more intermediate levels are possible by reducing the programming current interval.

Figure 5 shows the device resistance change induced by current pulses up to 1 mA in 0.1 mA increments. Nine distinct resistance levels were demonstrated here. It can be observed that the device resistance can be well controlled by applied electrical pulses.

The multilevel storage in the LTH-PCM device can be explained using the diagrams and corresponding equivalent circuits in Fig. 6. Here, we take four-level storage (e.g., two intermediate resistance levels) as an example. The device resistance R0 ("0") is the highest resistance level when the phase change (PC) layer is completely in the amorphous phase, as shown in Fig. 6(a). The equivalent circuit of the highest level is shown in Fig. 6(e). When applying an increasing current to the device, the resistance r_1 at steps in the PC layer, as shown in Fig. 6(b), firstly changes from r_{1a} to r_{1c} owing to the high electric field at the steps.[10] Previous experimental results revealed that the crystallization locally happened via its initial filament formation when the electric field across the PC layer reached its threshold value.[19,20] A sudden resistance drop can be observed in Figs. 4 and 5 after the application of around 0.3 mA caused by this phenomenon. As a result, device resistance drops from R0 (or "0") to R1 (or "1"). R0 and R1 correspond to the cases shown in Figs. 6(a) and 6(b). Then, the current flows through one electrode, one PC step, the top heater, another PC step, and another electrode, as shown in Fig. 6(b). The generated Joule heat dissipates, increases the temperature of the layer surrounded by these parts, and this layer crystallizes. The resistance of this layer is r_2, as shown in Fig. 6(c). The crystallization of this layer reduces the resistance r_2 from r_{2a} to r_{2c} owing to Joule heating. The resistances r_{2a} and r_{2c} correspond to the amorphous and crystalline phases of this layer, respectively. Correspondingly, device resistance decreases from R1 [or "1", Fig. 6(b)] to R2 [or "2", Fig. 6(c)]. Similarly, the higher current flows through the path, as

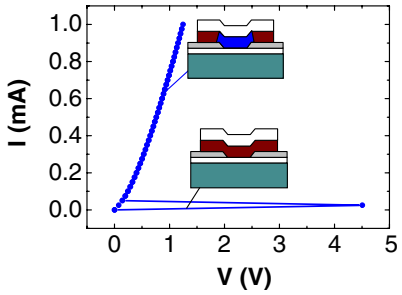

Fig. 7. (Color online) No gradual switching can be observed for the device without a top heating layer.

shown in Fig. 6(c), and the generated Joule heat increases the temperature of the layer shown as r_3 in Fig. 6(d) and it crystallizes. The resistances r_{3a} and r_{3c} correspond to the amorphous and crystalline phases of this layer, respectively. Correspondingly, the device resistance decreases from R2 [or "2", Fig. 6(c)] to R3 [or "3", Fig. 6(d)]. Consequently, four resistance levels are obtained owing to Joule heating, as described above. Obviously, the crystallization process from the top heater can be well controlled by the current applied for programming because the programmed area is determined by the Joule heat generated by the applied current. Thus, the crystallization between electrodes can gradually occur if we increase the applied current with a small increment. Gradual crystallization processes, therefore, create several of intermediate resistance levels, much more than two, as shown in Fig. 6.

Although the size of the device reported here is as large as 400–2000 nm, the shrinkability of the LTH-PCM device is expected to be good on the basis of the principle of the device in this work. With the decrease in the size of the device, the energy required for phase change (e.g., crystallization) becomes small. Furthermore, some improvements, such as adopting a bridge lateral structure with a top layer, are proposed. The excellent scalability of the bridge structure has been demonstrated by Chen *et al.*[3] The scalability of the LTH-PCM device is under investigation by both finite element analysis and experiment in our group.

The TiN layer plays a critical role in the device during programming. It changes the current path between electrodes and facilitates the electric field concentration. The subsequent Joule heating from the TiN layer leads to the initial enlargement of the crystalline zone. The role of TiN for MLS can be known from Fig. 7. The device without a top TiN heating layer did not exhibit the gradual switching by Joule heating. Crystallization suddenly occurs when the electric field between electrodes becomes higher than the threshold electric field of SbTeN in the device.

5. Conclusions

A lateral phase change memory with an additional top heating layer (LTH-PCM) was investigated for MLS. The active layers consist of a 50-nm-thick TiN layer as a top heater and a 150-nm-thick N-doped Sb_2Te_3 layer. Experimental results indicate that a number of intermediate levels, which are induced by electric currents, are distinct and stable. The multilevel storage results mainly from the gradual enlargement of the crystalline region and the increase in crystallinity between electrodes by Joule heating.

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